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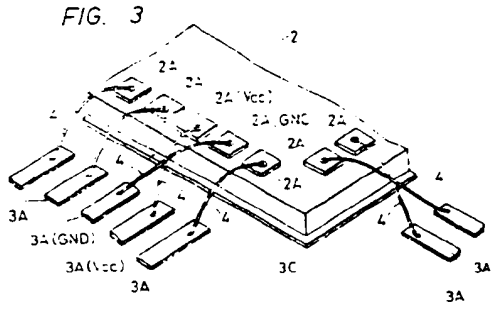
The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(54) Semiconductor chip having external terminals connected to corresponding leads by wires.

(57) A resin-encapsulated integrated circuit has a semiconductor chip (2) whose bonding pads (2A) are connected to corresponding leads (3A) by wires (4). In order to achieve the correct interconnection of pads (2A) and leads (3A) some of the wires (4) intersect and to prevent short circuits they are coated in an insulator. This permits great design versatility as the pads and leads may be positioned as desired, rather than having interconnected pads and leads adjacent each other, as is normal.

The use of insulated wires also permits one or more of the bonding pads to be central on the chip rather than at its periphery, and some of the pads may be connected to remote leads.

FIG. 3



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the optimum position to substantially equalize the lengths of wiring lines for connecting the timing signal generator circuit and various circuits.

Claims

1. A semiconductor device having external terminals of a semiconductor chip and leads or wiring lines formed on a circuit board for mounting the semiconductor chip thereon are connected by wires; wherein the wires are metal coated with an insulator, the external terminals of the semiconductor chip and the leads or the wiring lines are connected such that at least one of the wires intersects an adjacent wire.

2. A semiconductor device according to claim 1, in which the wires intersect so that the function of the lead or the wiring line can be altered without changing the arrangement of the external terminals of the semiconductor chip.

3. A semiconductor device having external terminals of a semiconductor chip and leads or wiring lines formed on a circuit board for mounting the semiconductor chip thereon are connected by wires; wherein a predetermined one of said external terminals is constructed at a central part of said semiconductor chip, that said wires are pieces of a coated wire in which a surface of a metal wire is coated with an insulator, and that one end of a piece of said coated wire is joined to said external terminal constructed centrally of said semiconductor chip, while the other end thereof is joined to the lead or the wiring line.

4. A semiconductor device as defined in Claim 3, characterized in that said semiconductor chip constructs a microcomputer, and that said external terminal arranged centrally is an external terminal which is connected to a timing generator circuit.

5. A semiconductor integrated circuit device comprising:

(a) a semiconductor integrated circuit chip which has first and second principal surfaces;

(b) a large number of bonding pads which are formed on said first principal surface;

(c) a resin mold member in which said chip and said pads are encapsulated;

(d) leads in a large number of at least 10 to 200, each of which includes an inner lead and an outer lead continuous thereto,

said each inner lead lying within said mold member, with said each outer lead protruding from said mold member; and

(e) bonding wires which respectively connect the inner leads of said leads and said pads corresponding thereto,

said wires being encapsulated in said resin mold member;

wherein at least one of said wires is formed with an insulator film over a whole circumference of a substantially full length thereof, and it is wire-bonded so as to intersect at least one of the other wires with respect to an orthogonal projection on said principal surface of said chip.

6. A semiconductor integrated circuit device as defined in Claim 5, wherein each of the other wires is formed with an insulator film over a whole circumference of a substantially full length thereof.

7. A semiconductor integrated circuit device as defined in Claim 6, wherein each of the large number of wires is subjected to ball wedge bonding.

8. A semiconductor integrated circuit device as defined in Claim 7, wherein said mold member is formed by transfer molding.

9. A semiconductor integrated circuit device as defined in Claim 8, wherein said insulator film as a coating of said each wire is removed at and near a part of said wire to be connected to the corresponding lead or pad, during a bonding process.

10. A semiconductor integrated circuit device as defined in Claim 9, wherein said coating consists principally of an organic resin.

11. A semiconductor device comprising:

(a) a semiconductor chip which has first and second principal surfaces;

(b) internal logic circuits which occupy a considerable area on said first principal surface of said chip;

(c) bonding pads in a large number of at least 50 to 200, which are disposed along peripheral sides of said chip,

said large number of pads including a first set, each element of which has a first function, and a second set, each element of which has a second function;

(d) leads in the large number of at least 50 to 200, which are so disposed that first ends thereof lie near outer sides of said peripheral sides of said chip;

(e) bonding wires in the large number of at least 50 to 200, which respectively connect said leads and the corresponding pads; and

(f) a resin mold member which encapsulates said chip, said wires, and said first ends of said leads as well as vicinities thereof;

wherein the first pad set of said first function is arrayed substantially in succession along each side of said chip, and when a small number of elements within the second pad set are inserted in said first pad set, these pads of said second function and the corresponding leads at positions remote therfrom are bonded by pieces of an insulator-coated wire.

12. A semiconductor device as defined in Claim 11, wherein said chip constructs a gate array IC.

13. A semiconductor device as defined in Claim 12, wherein each of said pads of said first function is one of an output pad and an input pad, while each of said pads of said second function is the other of them.

14. A semiconductor device as defined in

Claim 13, wherein said resin mold member is formed by transfer molding.

15. A semiconductor integrated circuit microcomputer device comprising:

(a) a first semiconductor chip on which at least one CPU is packaged, and which has first and second principal surfaces, an integrated circuit being formed on said first principal surface;

(b) at least one first bonding pad which is formed on a central or inner zone distant from peripheral sides on said first principal surface of said chip;

(c) second bonding pads in a large number of at least 10 to 200, which are disposed on said first principal surface of said chip;

(d) leads in the large number of at least 10 to 200, which are so disposed that first ends thereof lie near said peripheral sides of said chip;

(e) bonding wires in the large number of at least 10 to 200, which respectively connect said first ends of said leads and the corresponding second pads;

(f) a coating bonding wire which connects any one of said first ends of said leads and the corresponding first pad; and

(g) a resin mold member which encapsulates said chip, said first ends of said leads, said bonding wires, and said coated bonding wire.

16. A semiconductor integrated circuit microcomputer device as defined in Claim 15, wherein said mold member is formed by transfer molding.

17. A semiconductor integrated circuit microcomputer device as defined in Claim 16, wherein said first pad is an output terminal for clock pulses from a clock pulse generator circuit.

18. A semiconductor integrated circuit microcomputer device as defined in Claim 17, wherein said coated wire has an insulator film which extends substantially a whole surface thereof except bonding parts thereof.

19. A semiconductor integrated circuit microcomputer device as defined in Claim 18, wherein said bonding parts having been coated with the insulator film have said insulator film removed therefrom during a bonding process.

20. A resin-encapsulated semiconductor integrated circuit microcomputer device including first and second CPU chips within a single resin mold member, comprising:

(a) a system clock generator circuit which is provided on said first CPU chip;

(b) a clock output pad which is disposed on said first CPU chip in order to deliver a clock signal of said system clock generator circuit;

(c) a clock input pad which is disposed on said second CPU chip in order to introduce the system clock; and

(d) a bonding wire which connects said clock output and input pads.

21. A resin-encapsulated semiconductor integrated circuit microcomputer device as defined in Claim 20, wherein said wire is an insulator-coated wire.

22. A resin-encapsulated semiconductor integrated circuit microcomputer device as defined in Claim 21, wherein said wire is joined to said output pad on said first CPU chip by ball bonding and is joined to said input pad on said second CPU chip by wedge bonding.

23. A semiconductor integrated circuit memory device comprising:

(a) a memory chip in the shape of a rectangular plate, which has first and second principal surfaces and which has first and second shorter sides and first and second longer sides;

(b) at least one memory mat which occupies substantially a whole central area of said first principal surface of said chip;

(c) a first power source pad corresponding to either of a supply voltage V_{cc} and a reference voltage V_{ss}, which is disposed near said first shorter side on said first principal surface of said chip;

(d) a second power source pad corresponding to said either voltage, which is disposed near said second shorter side on said first principal surface of said chip;

(e) a resin mold member which is substantially in the shape of a rectangular parallelepiped of comparatively small height, and in which said chip is encapsulated,

said mold member having first and second opposing principal surfaces and having first and second opposing longer side surfaces and first and second opposing shorter side surfaces, said chip being located substantially centrally of said mold member so that said first principal surface of said chip becomes substantially parallel to said first principal surface of said mold member, that said first longer side of said chip becomes substantially parallel to said first longer side surface of said mold member, and that said first longer side of said chip and said first longer side surface of said mold member lie near to each other over a substantially full length of the former;

(f) a plurality of leads each of which includes an outer lead and an inner lead continuous thereto,

the respective outer leads of said leads protruding from said first longer side surface of said mold member substantially at equal intervals while forming a queue in a longitudinal direction thereof, the respective inner leads of said leads being encapsulated in said mold member; and

(g) at most two pieces of insulator-coated wire through which one of said inner leads is connected to both said first

and second power source pads,

said pieces of wire being encapsulated in said resin mold member.

24. A semiconductor integrated circuit memory device as defined in Claim 23, wherein said chip is not underlaid with a single tab of large area for fastening said chip thereon.

25. A semiconductor integrated circuit memory device as defined in Claim 24, wherein said chip has said second principal surface thereof fastened on the plurality of inner leads through an insulator film member.

26. A semiconductor integrated circuit memory device as defined in Claim 23, wherein said chip is a DRAM chip.

27. A semiconductor integrated circuit memory device as defined in Claim 23, wherein said one inner lead is branched at its inner end, and said at most two pieces of coated wire are bonded at the branched end parts.

28. A semiconductor integrated circuit memory device as defined in Claim 23, wherein said resin mold member is formed by transfer molding.

29. A method of manufacturing a semiconductor device, comprising:

(a) the step of fastening a semiconductor pellet onto a lead frame;

(b) the step of connecting bonding parts of said lead frame and corresponding pads on said pellet by the use of bonding wires;

(c) the step of encapsulating said pellet, said bonding parts of said lead frame and said bonding wires with a resin; and

(d) the step of separating the resin mold member from a body of said lead frame;

wherein those of said bonding wires which are liable to short-circuit at, at least, the resin molding step in case of bonding said bonding wires in accordance with a desired specification without changing a layout of said lead frame are formed of pieces of insulator-coated wire.

30. A method of manufacturing a semiconductor device as defined in Claim 29, wherein all of said bonding wires are of said insulator-coated wire.

31. A method of manufacturing a semiconductor device as defined in Claim 30, wherein said pellet constructs a gate array.

32. A method of manufacturing a semiconductor device as defined in Claim 30, wherein each of said bonding wires is formed with an organic coating over its full length in advance, and parts of said coating corresponding to bonding points are removed during the bonding step.

33. A method of manufacturing a semiconductor device as defined in Claim 32, wherein said pellet constructs a CPU of a microcomputer.

34. A method of manufacturing a semiconductor device as defined in Claim 32, wherein said pellet constructs a DRAM chip.

35. A method of manufacturing a semiconductor device as defined in Claim 32, wherein said bonding wires consist essentially of copper.

FIG. 1

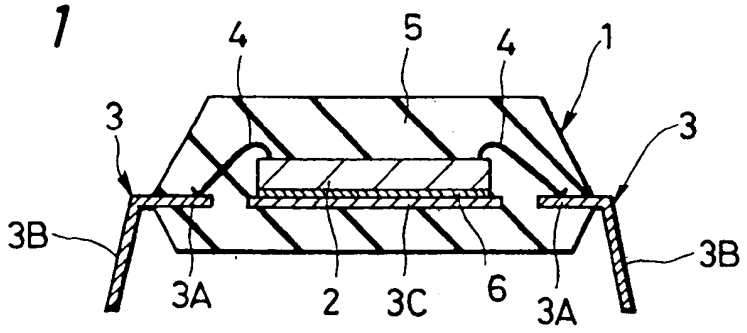


FIG. 2

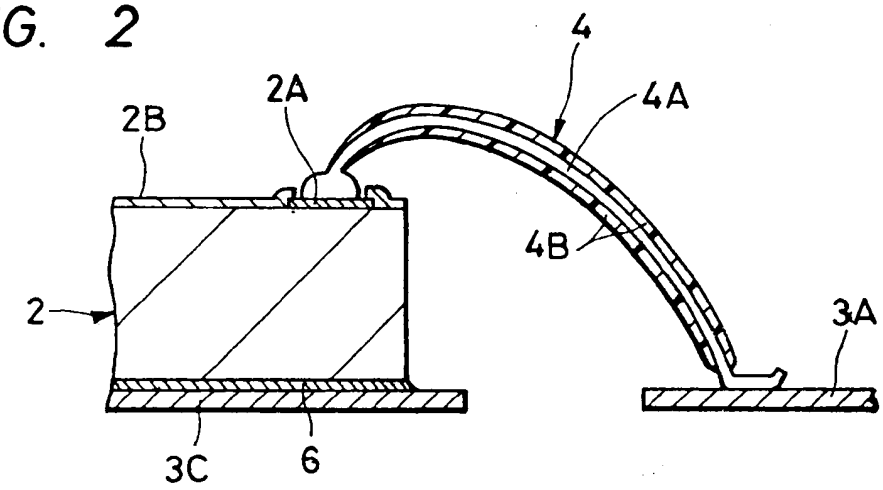


FIG. 3

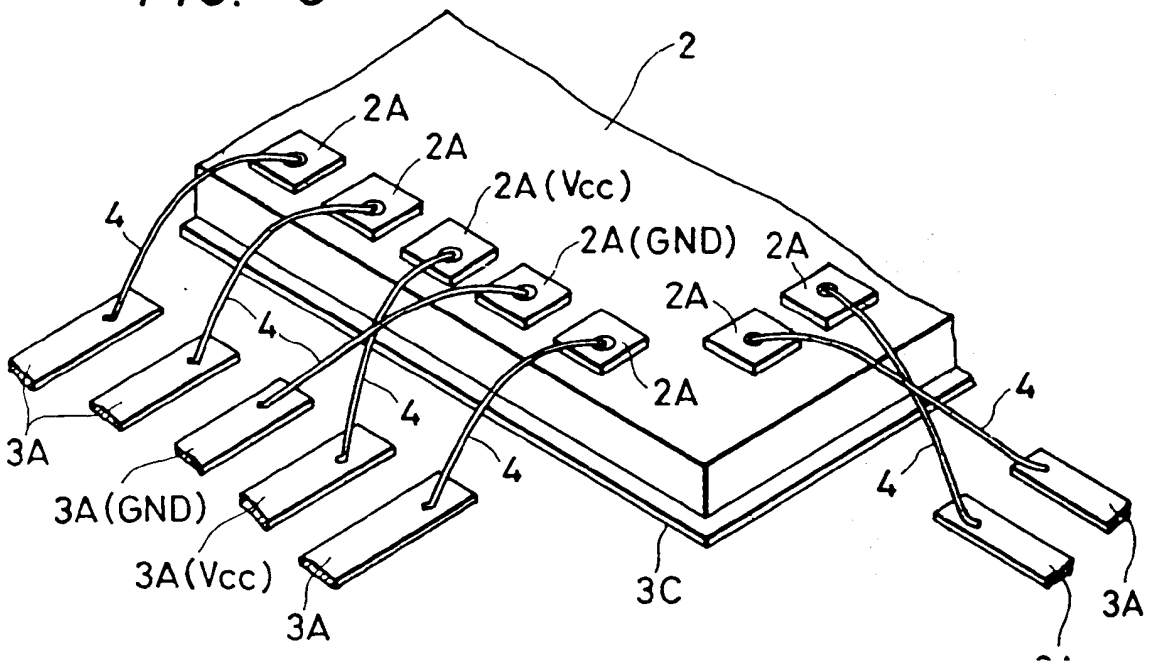


FIG. 4

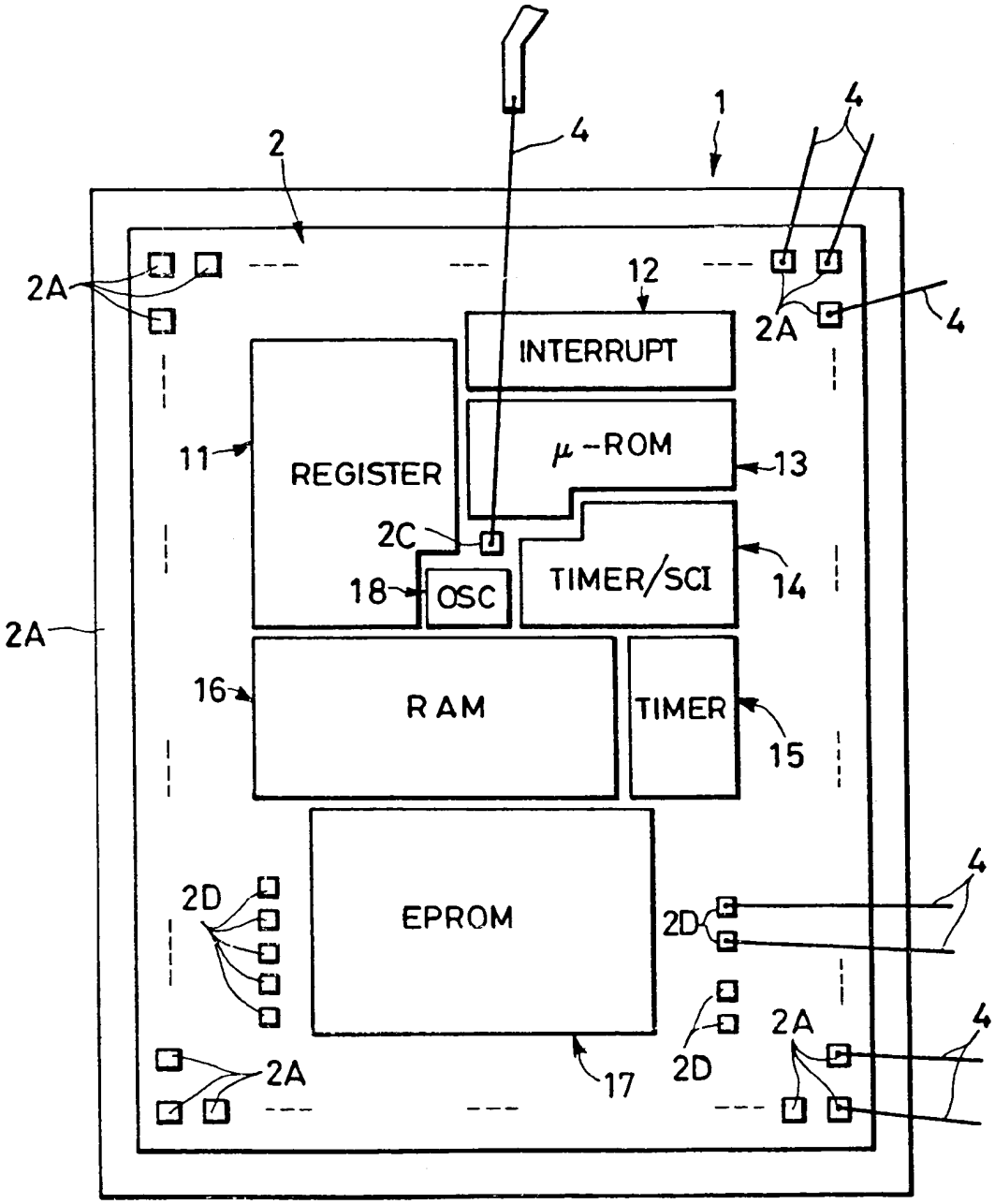

1
2
4
4
2A
12
INTERRUPT
2A
4
11
REGISTER
μ-ROM
13
2C
18
OSC
TIMER/SCI
14
2A
16
RAM
TIMER
15
2D
EPROM
4
2D
2D
2A
4
2A
17

FIG. 5

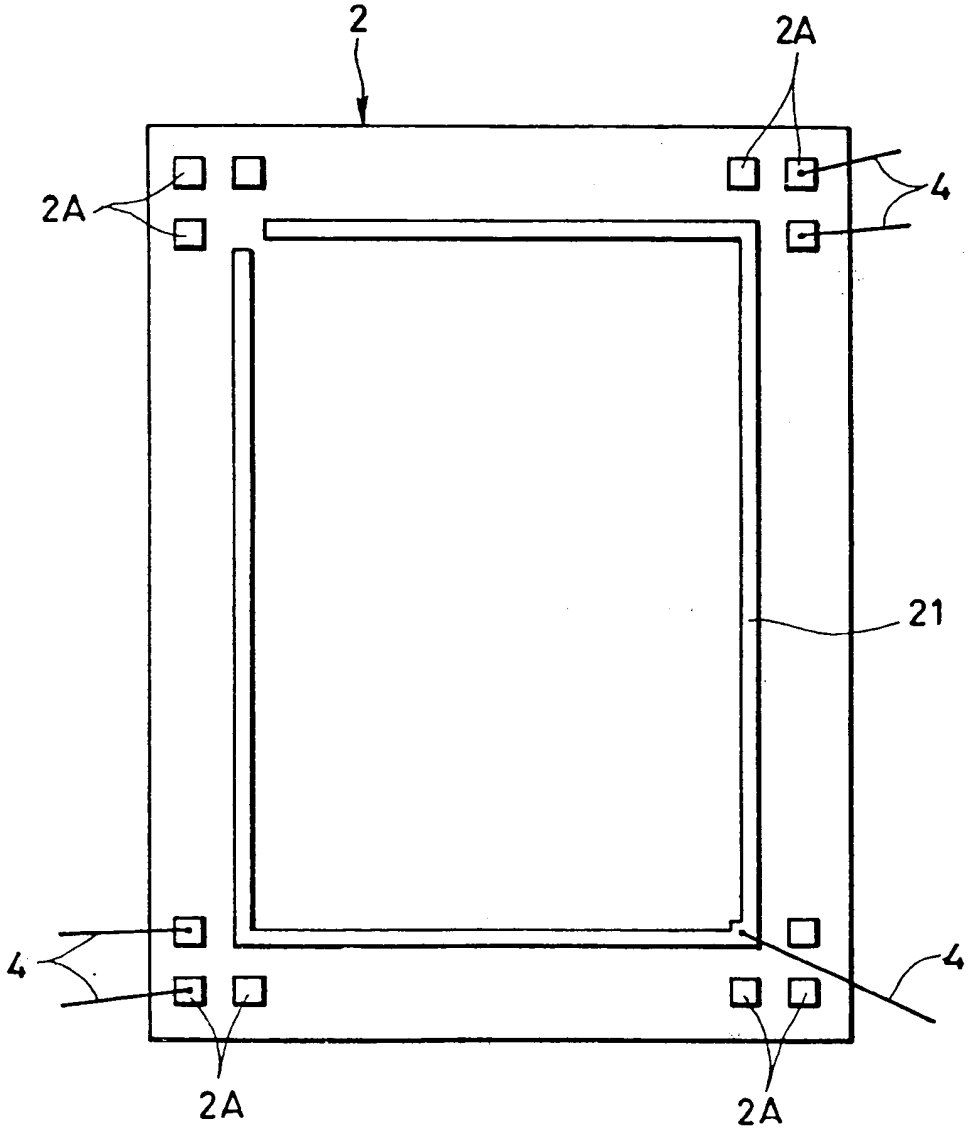


FIG. 9(a)

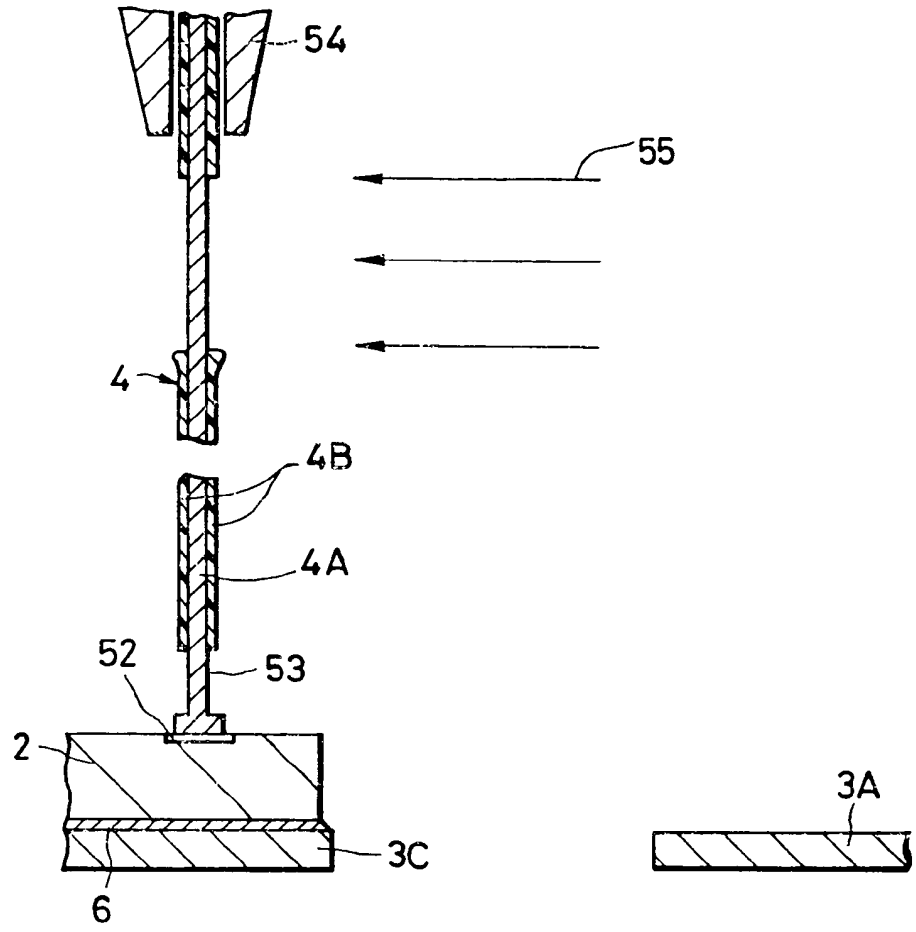
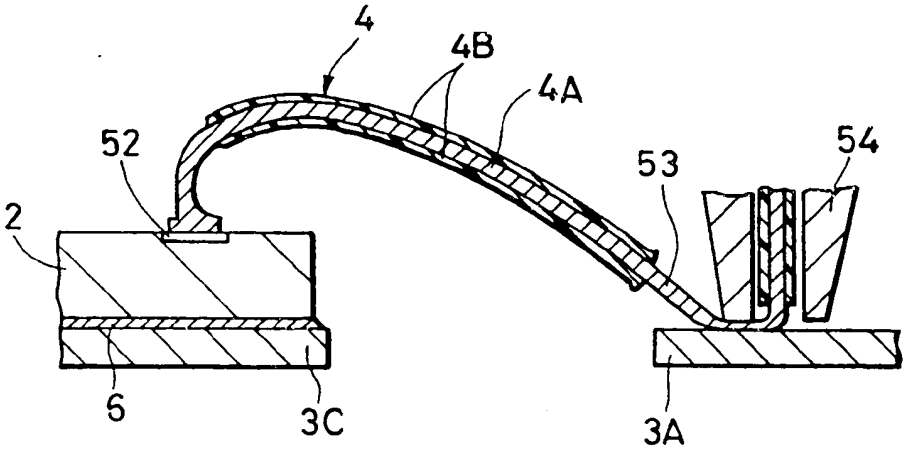


FIG. 9(b)



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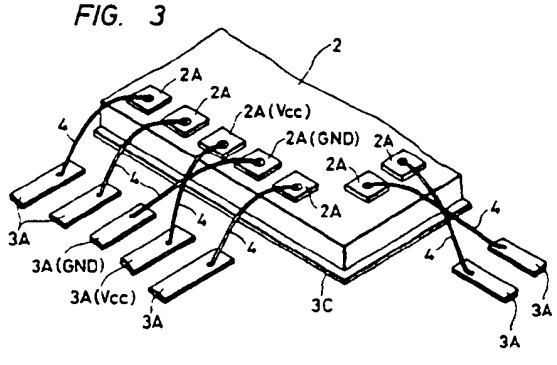

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EUROPEAN SEARCH REPORT

Application Number

EP 88 30 0399

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y,A	PATENT ABSTRACTS OF JAPAN, vol. 10, no. 376 (E-464)[2433], 13th December 1986; & JP-A-61 168 949 (TOSHIBA) * Abstract *	1	H 01 L 23/48 H 01 L 21/60
Y	US-A-3 969 752 (POWER HYBRIDS) * Figures 1,2 *	1	
A		3	
A	DE-A-3 244 323 (HITACHI) * Figure 4; claims 1,6 *	7	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)
H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	05-03-1990	DE RAEVE R.A.L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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